REMARKS

After the foregoing amendments, claims 1, 3-5, 7-10, and 12-15 are active in the present application.

We acknowledge the Examiner's indication that claims 1 and 3-5 are allowed. However, we have amended independent claim 1 to correct a minor typographical error and to add a feature relating to restarting timing of data recording. We also acknowledge the Examiner's indication that claims 7-10 and 12-15 would be allowable if rewritten in independent form and to include all of the features of the base and intervening claims. Accordingly, we have amended dependent claims 7 and 12 to be in independent form and to correct minor typographical errors. We have also cancelled claims 6 and 12.

The amendments are supported by the specification from page 20, line 29 to page 21, lines 20 of the specification and Fig. 3. More specifically, in certain embodiments, the clock generator 15 generates a first system clock SCK1 and a second system clock SCK2 in the following manner:

When the decoding of the decoder is delayed from the encoding of the encoder, the clock generator 15 suspends providing the first system clock SCK1 to the encoder 14 until the decoding of the decoder 7 catches up with the encoding of the encoder 14. This feature is illustrated in Fig. 3 as "clock stop." Encoding of the encoder 14 and decoding of the decoder 7 are synchronized at a timing just before Sk and Ak of Fig. 3. At this timing, the clock generator 15 restarts providing the first system clock SCK1 to the encoder 14. From when decoding of the decoder 7 and encoding of the encoder 14 reach the data at which data recording was interrupted (just after Sn and An of Fig. 3), the clock generator 15 provides the second system clock SCK 2 to the encoder 14 instead of the first system clock SCK1. Accordingly, the writing of data can be restarted from the interruption position (just after An) in a manner that the continuity of the data is ensured.

None of the cited prior art, including Shinada, discloses or suggests providing a second system clock to an encoder, when decoding of a decoder and encoding of the encoder reach the data at which data recording was interrupted. We submit that because claims 3-5 depend from

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independent claim 1, claims 8-10 depend from claim 7, and claims 13-15 depend from independent claim 12, these dependent claims are allowable for at least the same reasons that independent claims 1, 7 and 12 are allowable.

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Respectfully submitted,

Date: February 2, 2004

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